WHAT IS CLAIMED IS:

1. A method comprising:

providing a first processor on a single silicon chip; loading, on the first processor, a software simulation of a second processor that is to be provided in hardware on the single silicon chip;

loading, on the first processor, an applications software that is to be executed on the hardware of the second processor; and

executing the software simulation of the second processor and the applications software on the first processor.

2. The method of claim 1:

wherein the software simulation of the second processor includes a slow, highly detailed simulation of the second processor and a fast, high-level simulation of the second processor;

and further comprising selecting the software simulation as either the slow, highly detailed simulation or the fast, high-level simulation.

3. The method of claim 2 wherein the slow, highly detailed simulation of the second processor includes a

simulation of bus interface to the second processor and to memory and control status registers.

4. The method of claim 1 wherein:

said loading, on the first processor, a simulation of a second processor that is to be provided in hardware on the single silicon chip includes loading, on the first processor, a plurality of software simulations of a plurality of second processors that are to be provided in hardware on the single silicon chip, each software simulation corresponding to one of the second processors.

5. The method of claim 4 wherein:

said loading, on the first processor, an applications software that is to be executed on the hardware of the second processor includes loading, on the first processor, a plurality of applications software, each applications software to be executed on the hardware of a corresponding one of the plurality of second processors.

6. The method of claim 5 wherein:

said executing the software simulation of the second processor and the applications software on the first processor includes executing the plurality of software

simulations of the plurality of second processors and the plurality of applications software on the first processor.

7. The method of claim 4:

wherein each software simulation of the second processors includes a slow, highly detailed software simulation of second processor and a fast, high-level simulation of the second processor;

and further comprising selecting each software simulation as either the slow, highly detailed simulation or the fast, high-level simulation.

8. The method of claim 1 further comprising:

providing a third processor external to the single silicon chip;

wherein the software simulation of the second processor includes a first interface;

configuring the first interface to execute the software simulation of the second processor on the third processor;

loading, on the third processor, the software simulation of the second processor;

wherein the applications software includes a second interface;

configuring the second interface to execute the applications software on the third processor;

loading, on the third processor, the applications software; and

executing the software simulation of the second processor and the applications software on the third processor.

9. The method of claim 1 further comprising:

providing the second processor as hardware on the single silicon chip;

wherein the applications software includes an interface;

configuring the interface to execute the applications software on the hardware of the second processor; and

executing the applications software on the hardware of the second processor.

10. A computer program product embodied on a tangible storage medium, the program comprising executable instructions that enable the computer to:

configure a software simulation of a first processor, which is to be provided in hardware on a single silicon chip, to execute on a second processor on the single

silicon chip in either a slow, highly detailed simulation mode or a fast, high-level simulation mode; and

configure a first applications software, which is to be executed on the hardware of the first processor, to execute with the software simulation of the first processor on the second processor or to execute on the hardware of the first processor.

11. The computer program product embodied on a tangible storage medium of claim 10, the program further comprising executable instructions that enable the computer to:

configure a second applications software to execute on either the second processor or a processor external to the single silicon chip.

12. A method of developing software for a multi-processor chip, the method comprising:

loading, on a first processor, a plurality of software simulations of a plurality of second processors that are to be provided in hardware on a single silicon chip, each software simulation corresponding to a one of the second processors, and each software simulation includes a slow, highly detailed simulation of the second processor and a fast, high-level simulation of the second processor;

selecting each software simulation as either the slow, highly detailed simulation or the fast, high-level simulation;

loading, on the first processor, a plurality of applications software, each applications software to be executed on the hardware of a corresponding one of the plurality of second processors; and

executing the plurality of software simulations of the plurality of second processors and the plurality of applications software on the first processor.

13. The method of claim 12 wherein the slow, highly detailed simulation of the second processor includes a simulation of bus interface to the first processor and to memory and control status registers.

14. The method of claim 12 further comprising providing the first processor as hardware on the single silicon chip.

15. The method of claim 12 further comprising providing the first processor as hardware external to the single silicon chip.

16. The method of claim 12 further comprising:

providing a one of the plurality of second processors as hardware on the single silicon chip;

wherein each of the plurality of applications software includes an interface;

configuring the interface of the applications software corresponding to the one of the plurality of the second processors to execute the applications software corresponding to the one of the plurality of the second processors on the hardware of the one of the plurality of second processors; and

executing the applications software on the hardware of the second processor.

17. An apparatus for developing software for a multi-processor chip comprising:

a first processor on a single silicon chip having loaded thereon,

a software simulation of a second processor that is to be provided in hardware on the single silicon chip, and

an applications software that is to be executed on the hardware of the second processor;

the first processor to execute the software simulation of the second processor and the applications software on the first processor.

18. The apparatus of claim 17 further comprising:

a third processor external to the single silicon chip having loaded thereon the software simulation of the second processor and the applications software;

the third processor to execute the software simulation of the second processor and the applications software.